REMARKS

Claims 5-8 and 10-12 are pending. Claims 5, 8 and 10 are independent and amended. Claims 1-4 are canceled.

Claim Rejections – 35 U.S.C. § 102

Claims 5-7 and 10-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Hirabayashi (U.S. Patent No. 5,614,445). Applicant respectfully traverses this rejection.

Hirabayashi discloses a semiconductor chip and fabrication method including the formation of element separation regions in a semiconductor substrate. As shown in Figures 1-4, an element separation area or scribe lane area 5 is formed by etching the substrate create dummy etch grooves 6.

Since the scribe lane area 5 is created by etching the substrate, Hirabayashi does not disclose, "said scribe lanes...containing only an unetched portion of the semiconductor substrate," as recited by claims 5 and 10 as amended.

Applicant respectfully submits that the term "only" limits the feature of the scribe lane to containing just the unetched portion of the semiconductor substrate. Contrary to the Examiner's assertions regarding the breadth of the term "comprising", "only" may be used as a modifying claim limitation.

Accordingly, claims 5-10 are allowable over the prior art. Regarding claims 6-7 and 11-12 these claims are allowable for at least the same reasons as their corresponding independent claims.

Therefore, Applicant respectfully requests removal of this rejection.

Claim Rejections – 35 U.S.C. § 103

Claim 8 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hirabayashi (U.S. Patent 5,614,445) in view of Kim et al. (U.S. Patent 6,159,826). Applicant respectfully traverses this rejection.

According to 103(c), Kim et al. does not qualify as prior art in the present application. Kim et al. is a 102(e) type reference used in a 103(a) rejection. Further, the present application was filed after November 29, 1999. Additionally, Kim et al. and the present application were at the time the present invention was made, subject to assignment to the same entity, Hyundai Electronics Industries Co., Ltd. As a result, the present rejection is improper under § 103(c), and claim 8 is allowable over the prior art.

Accordingly, Applicant respectfully requests withdrawal of this rejection.

CONCLUSION

The Examiner is respectfully requested to enter this Amendment After Final in that it raises no new issues and places the application in condition for

allowance, or in the alternative better form for Appeal. Early and favorable notice to that effect is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the application by this Amendment.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to contact Jayne Saydah (Reg. No. 48,796) at (703) 205-8000, in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment: Version With Markings Showing Changes Made

VERSION WITH MARKINGS SHOWNG CHANGES MADE

IN THE CLAIMS

Claims 1-4 are canceled.

The claims have been amended as follows:

5. (Twice Amended) A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes in the semiconductor substrate, said scribe lanes defining chip formation areas and containing only **an unetched portion of** the semiconductor substrate;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

forming at least one well area within the deep well area.

8. (Three Times Amended) **[The method of claim 5,] A method for manufacturing a semiconductor device comprising:**

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes in the semiconductor substrate, said scribe lanes defining chip formation areas;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

forming at least one well area within the deep well area,

wherein**[,]** the first conductivity type is a n-type conductor; and the second conductivity type is a p-type conductor.

10. (Three Times Amended) A method for manufacturing a semiconductor device comprising:

preparing a semiconductor substrate of a first conductivity type;

forming scribe lanes in the semiconductor substrate, said scribe lanes defining chip formation areas **and containing only an unetched portion of the semiconductor surface**;

forming a deep well area in each chip formation area, each deep well area having a second conductivity type opposite the first conductivity type; and

wherein a first conductive well area and a second conductive well area are separately formed within the deep well area,

the first conductive well area is formed of the first conductivity type, and

the second conductive well area is formed of the second conductivity type.